

Fig. 1

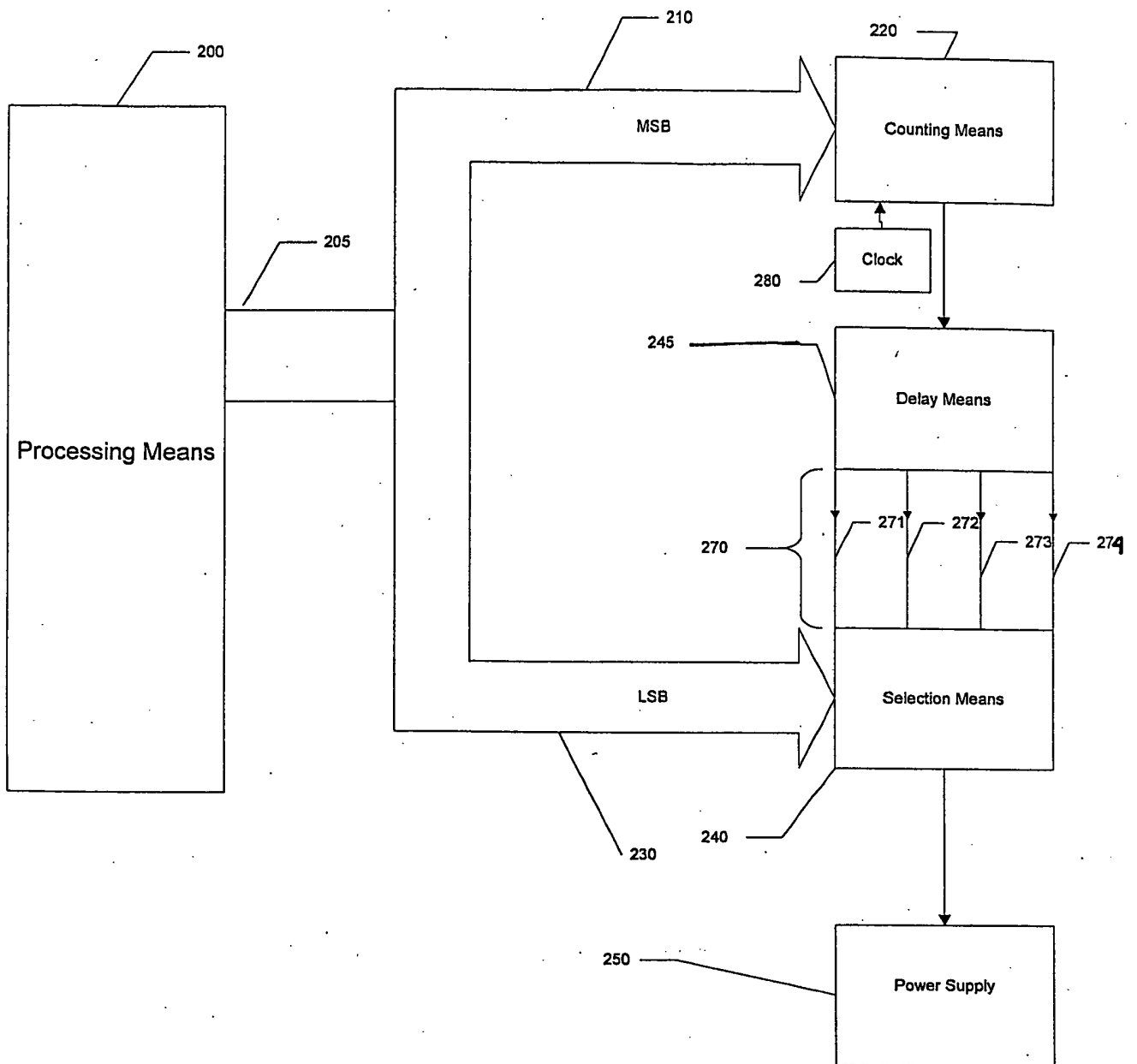
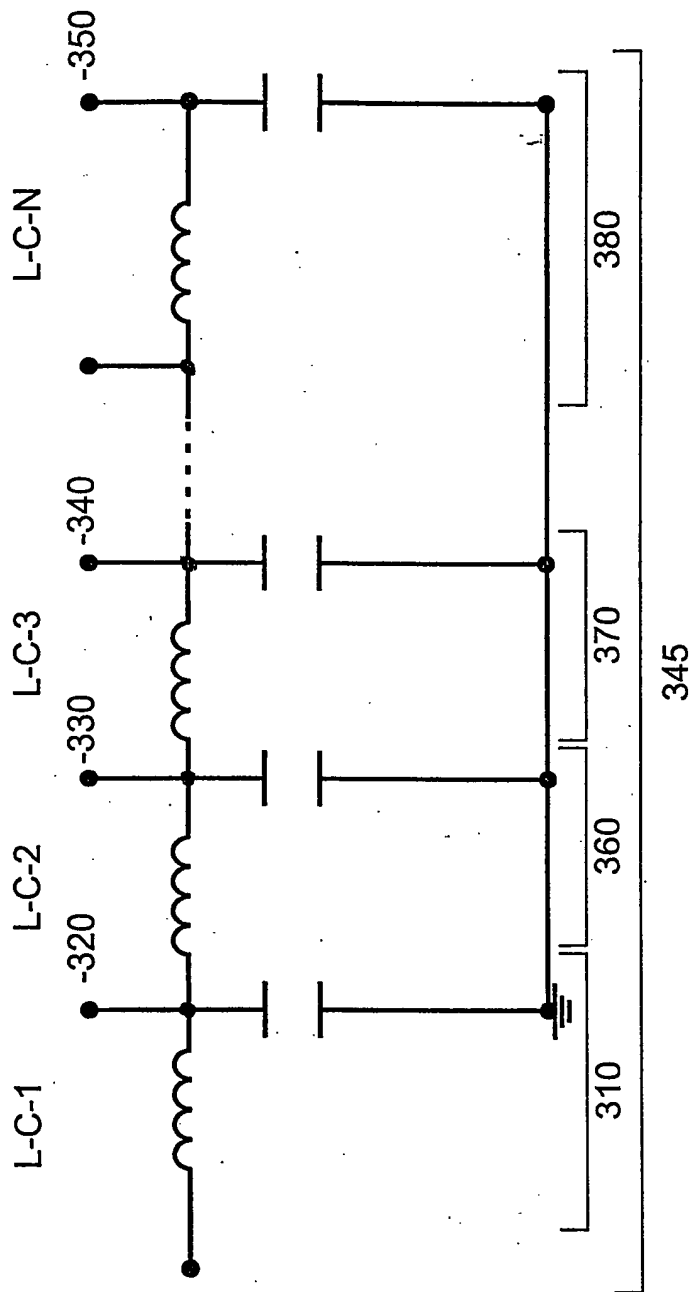


Fig. 2

Fig. 3

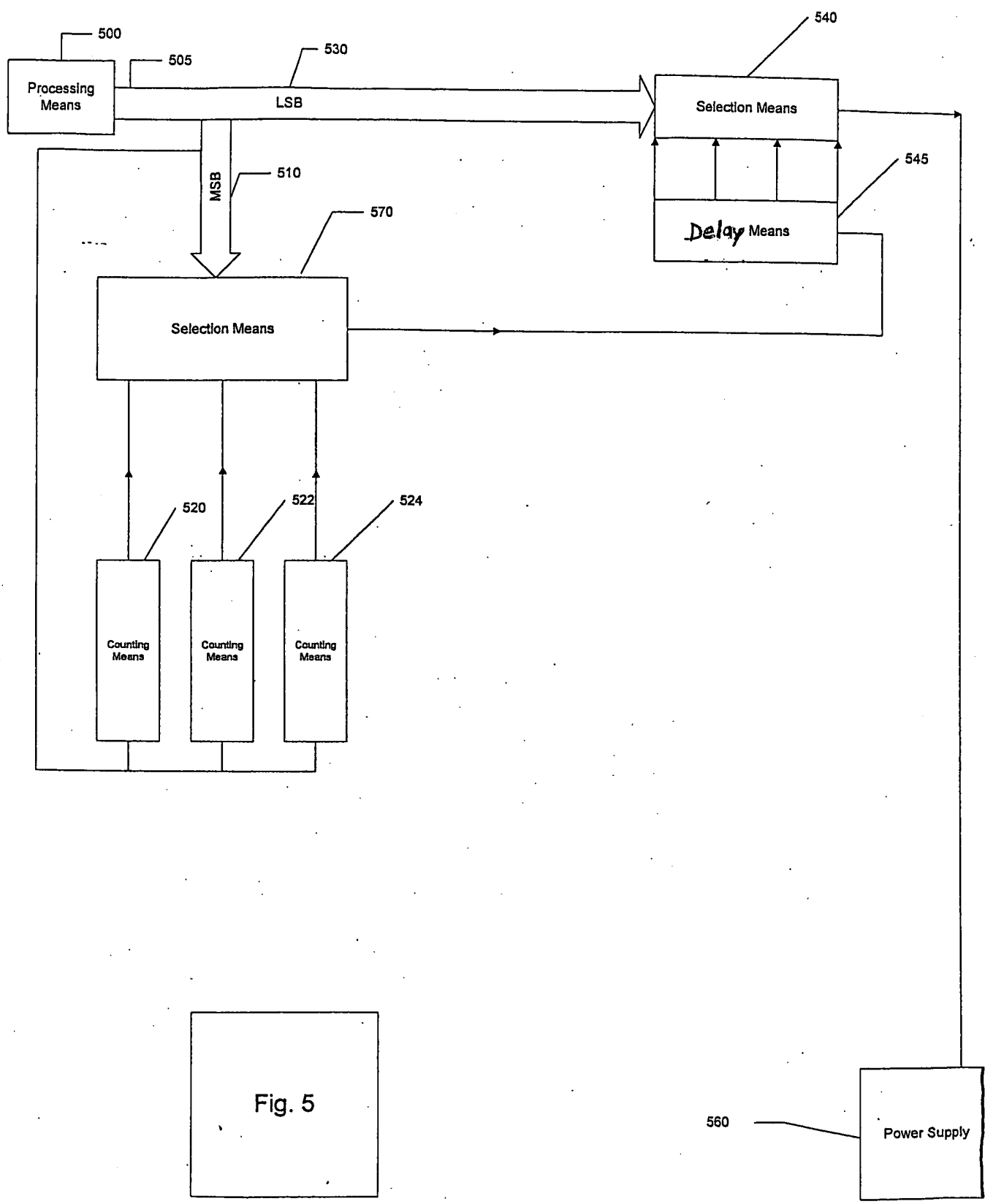


The diagram shows a system architecture with the following components and connections:

- Processor (400):** A large block on the left. It has a sub-component labeled **16.75 nanosecond** (405) connected to the **MSB - 16 nanoseconds** (410) input of the counter.
- Counter (420):** Labeled "Counter 8 nanoseconds time slices". It receives the **MSB - 16 nanoseconds** (410) signal from the processor and a **Clock 125 MHz** (480) signal. Its output goes to the **Delay Line** (445).
- Delay Line (445):** A block containing four segments labeled 471, 472, 473, and 474. Their respective values are .25, .50, .75, and 1.0. The output of the delay line goes to the **Multiplexor** (440).
- Multiplexor (440):** Receives input from the delay line and the **LSB - .75 nanoseconds** (430) signal from the processor. Its output is labeled 440.
- Power Supply (450):** Receives input from the multiplexor output (440).

Fig. 4

00000000-00000000



1990年12月31日

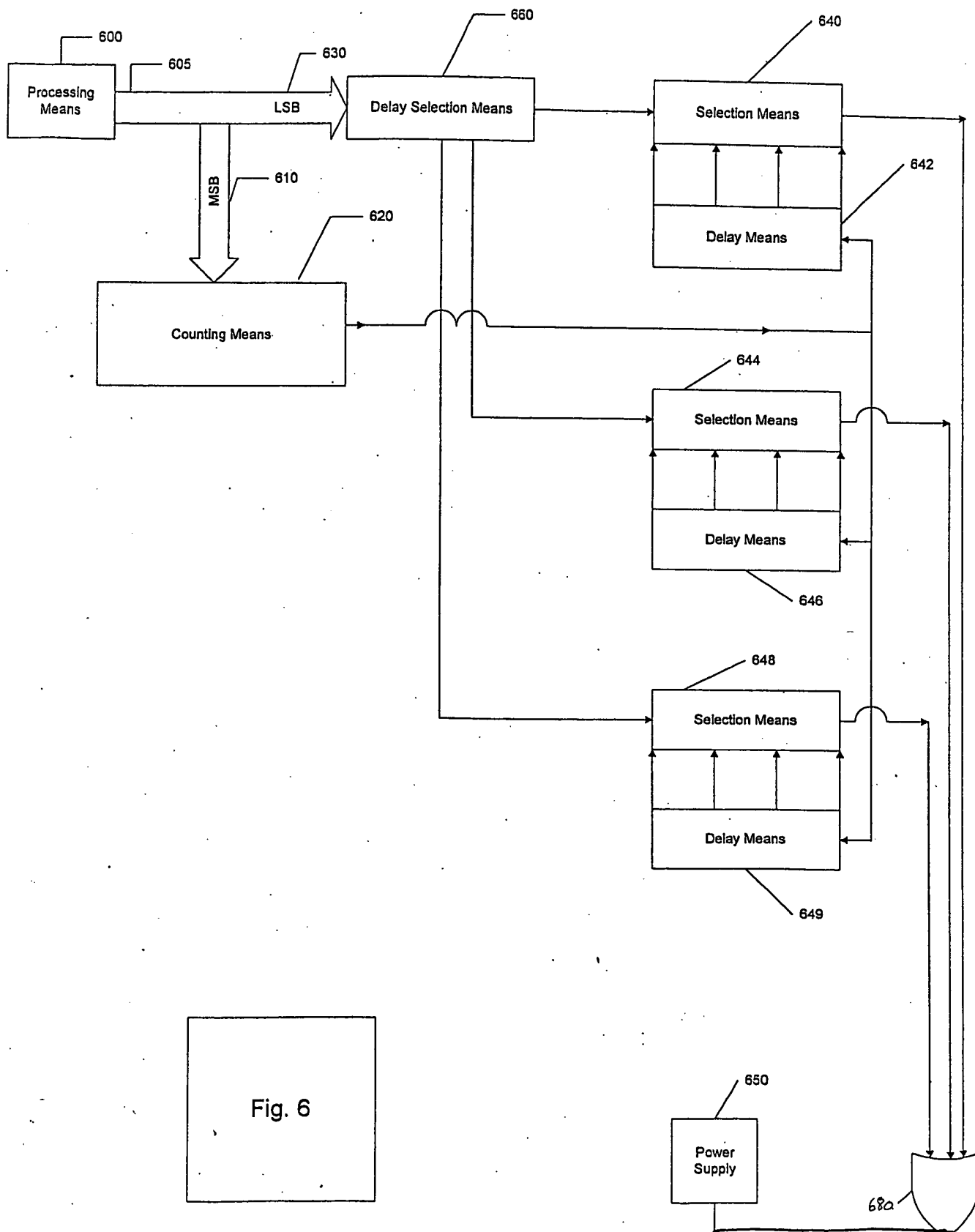
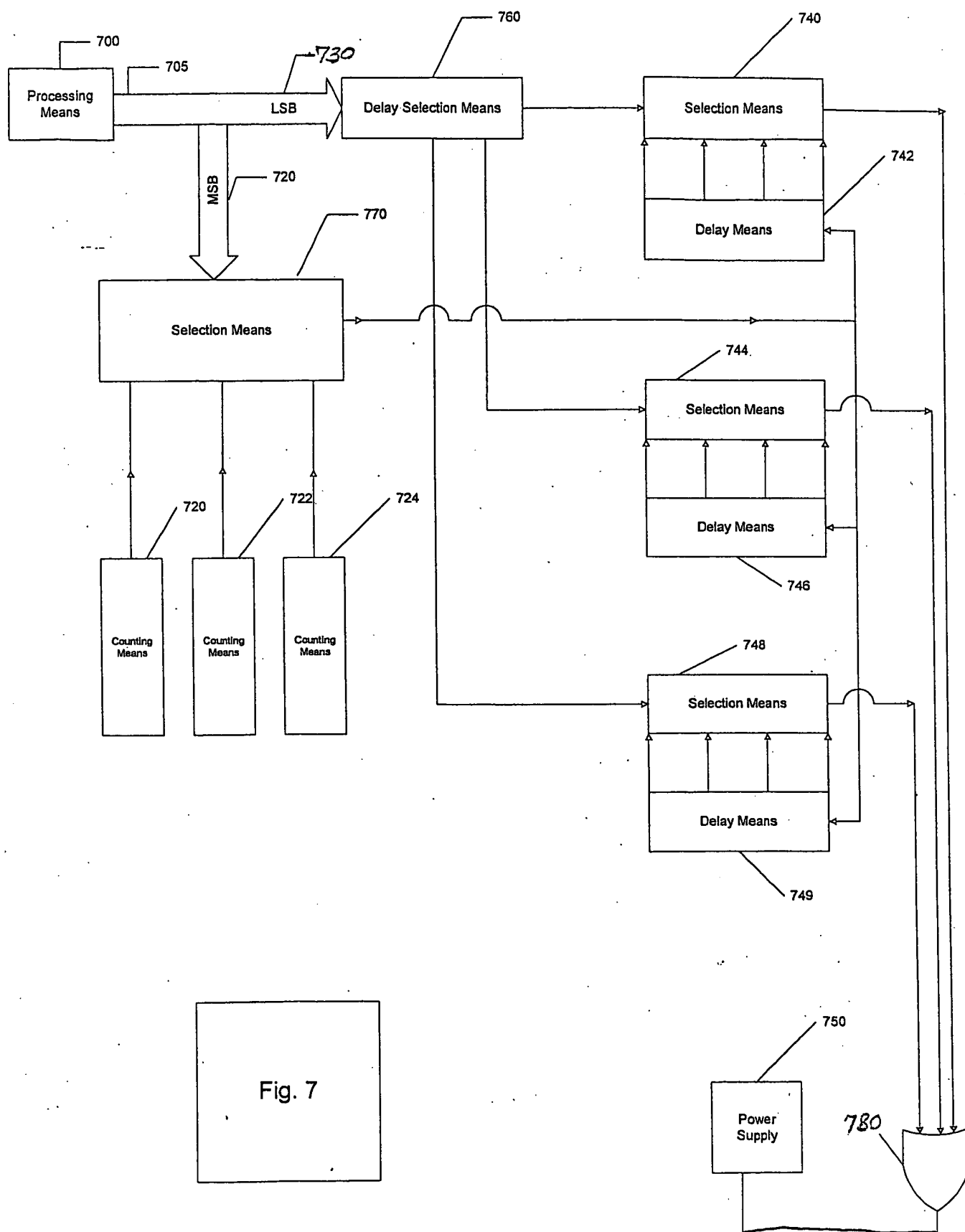


Fig. 6

CONFIDENTIAL



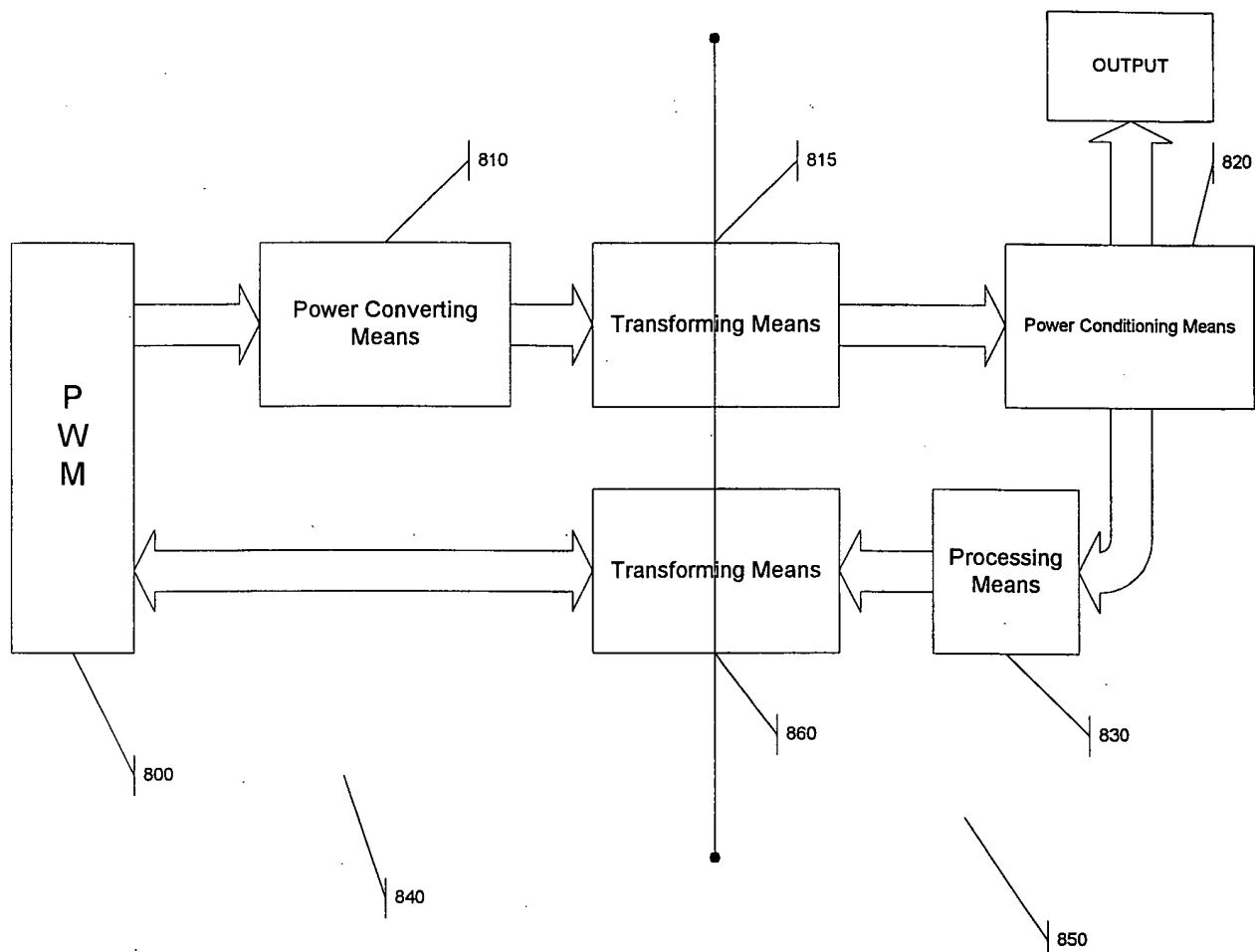


FIG. 8

THE JOURNAL OF THE

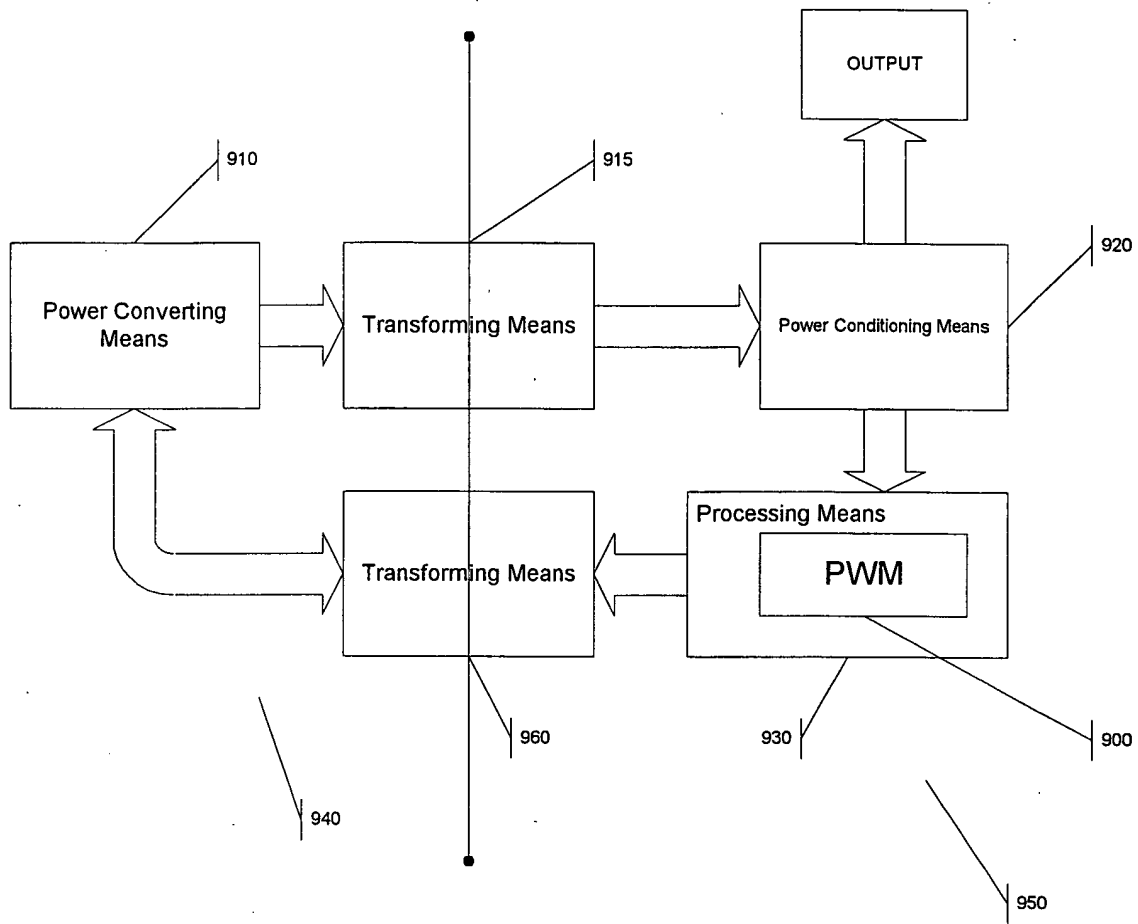


FIG. 9